The drawings were objected for failing to comply with 37 C.F.R. § 1.84(p)(5). Figs. 1 and 2 have been amended in response to the objection. Claim 12 was rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Claim 12 has been amended.

Claims 2 and 6-13 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hsu in view of Gill. Applicants respectfully traverse the rejection. Claim 2 has been canceled. Claim 6 recites, among other features, "wherein a specific floating gate transistor of the plurality is selected and programmed by applying a first voltage to the control gates of the transistors in the row in which the specific transistor is disposed, applying a second voltage to the source of the specific transistor and grounding the drain of the specific transistor."

The Examiner stated, on page 5, the first paragraph:

> ...it would have been obvious to one having ordinary skill in the art at the time the invention was made to bias the source, drain, and control electrode[s] to different means and for the programming of a cell as a matter of design choice to supply a current to the device.

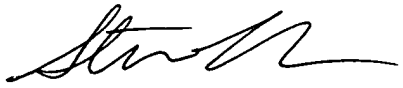
Applicants respectfully disagree. As explained in the background section, the word line (or control gate) and the bit line (or drain region) are provided with 8.5 volts and 4.5 volts, respectively, according to a conventional technique (page 2, third paragraph). However, the present inventors have discovered that a memory device having the features of claim 6 and programmed according to claim 6 provides significantly improved results (see, Figs. 6-9). Neither Hsu nor Gill discloses the above recited features. Therefore, claim 6 and its dependent claims are allowable at least for this reasons.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

On page 1, the sixth paragraph has been replaced with the following paragraph:

-- FIG. 1 shows a cell 10 with a control gate 12, a floating gate 14, a source 16 and a drain 18. Control gate 12 and floating gate 14 are separated from source 16 and drain 18, and from a substrate 11 [20] into which the source 16 and drain 18 are formed, by an oxide 22 which may be formed by one or more layers of a suitable oxide material. Suitable openings in the oxide 22 are provided to allow for external connection to source 16 and drain 18. As shown, connections are provided to set V_g (control gate voltage), V_d (drain voltage), V_s (source voltage) and V_b (substrate voltage). --

IN THE CLAIMS:

All pending claims have been provided below for the Examiner's convenience. The claims have been amended as indicated below:

Claims 1 through 5 have been cancelled.

6. A flash memory, comprising:

a plurality of floating gate transistors, each transistor having a control gate a floating gate, a drain and a source, said plurality arranged in an N-row by M-column array, where N and M are integers greater than or equal to one;

N word lines, each word line connecting together the control gates of transistors in a common and corresponding row; and

M bit lines, each bit line connecting together the drains of transistors in a common and corresponding column,

wherein a specific floating gate transistor of the plurality is selected and programmed by applying a first voltage to the control gates of the transistors in the row in

which the specific transistor is disposed, applying a second voltage to the source of the specific transistor and grounding the drain of the specific transistor.

7. The flash memory of claim 6, wherein the sources of all transistors are connected together as a common source.

8. The flash memory of claim 6, wherein the second voltage is greater than ground potential.

9. The flash memory of claim 6, wherein the source of each transistor comprises a first doped region having a first conductivity type extending into a semiconductor substrate having a second conductivity type of a charge opposite to the first conductivity type, thereby forming a first p-n junction.

10. The flash memory of claim 9, wherein the drain of each transistor comprises a second doped region of the first conductivity type, which is laterally spaced from the first doped region and extends into the substrate, thereby forming a second p-n junction.

11. (Amended) The flash memory of claim 10, wherein the first doped region is a double-diffused region comprising a first sub-region of a first dopant species and a second sub-region of a second dopant species, the first and second dopant species being of the first conductivity type.

12. (Amended) The flash memory of claim 11, wherein the first doped region extends deeper into the substrate than the [first] second doped region.

13. The flash memory of claim 12, wherein the floating gate of each transistor is disposed vertically above and interposed between an oxide layer and the substrate such that the first doped region horizontally overlaps the floating gate to a greater extent than a horizontal overlap of the second doped region.

The following new claims have been added:

-- 14. (New) A non-volatile device, comprising:

a substrate;

a floating gate overlying the substrate;

a control gate overlying the floating gate and being electrically coupled to a word line extending in a first direction;

a drain region provided in the substrate and proximate a first end of the floating gate, the drain region extending into the substrate and having a first depth, the drain region having a first graded profile and being electrically coupled to a bit line extending in a second direction that is substantially perpendicular to the first direction; and

a source region provided in the substrate and proximate a second end of the floating gate, the source region and drain region defining a channel therebetween, the source region extending into the substrate and having a second depth that is greater than the first depth, the source region having a second graded profile that is more sloped than the first graded profile,

wherein the control gate is applied with a first voltage and the source region is applied with a second voltage to program the non-volatile device.

15. (New) The device of claim 14, wherein the drain region is grounded to program the non-volatile device.

16. (New) The device of claim 15, wherein the source region is a double-diffused region including first and second species.

17. (New) The device of claim 16, wherein the first species is arsenic and the second species is phosphorous.

18. (New) The device of claim 15, wherein the first voltage is about 8.5 volts and the second voltage is about 4.5 volts.

19. (New) A non-volatile semiconductor device, comprising:

a semiconductor substrate; and

a transistor formed on the substrate, the transistor including:

a floating gate overlying a surface of the substrate,

a control gate overlying the floating gate and being electrically coupled to a first conductive line extending in a first direction,

a first conductive region provided in the substrate and proximate a first end of the floating gate, the first conductive region extending a first distance into the substrate and having a first graded profile relative to the surface of the substrate, the first conductive region being electrically coupled to a second conductive line extending in a second direction that is substantially perpendicular to the first direction, and

a second conductive region provided in the substrate and proximate a second end of the floating gate, the second conductive region being a double-diffused region that extends a second distance into the substrate and having a second graded profile relative to the surface of the substrate, the second distance being greater than the first distance, the second graded profile having a greater slope relative to the surface of the substrate than the first graded profile,

wherein the control gate is applied with a first voltage and the second conductive region is applied with a second voltage to program the non-volatile device, the second voltage being a positive voltage.

20. (New) The device of claim 19, wherein the first conductive region is grounded to program the non-volatile device.

21. (New) The device of claim 19, wherein the transistor is one of a plurality of cells formed on the substrate, the plurality of cells being arranged in an array of N rows and M columns, each of the plurality of cells being configured to be programmed to a first conductive state or a second conductive state.

22. (New) The device of claim 19, wherein the second conductive region includes first and second species.

23. (New) The device of claim 22, wherein the first species is arsenic and the second species is phosphorous.

24. (New) The device of claim 19, wherein the first distance is about 0.1 micron and the second distance is about 0.3 micron.

25. (New) The device of claim 19, wherein the second distance is about three times greater than the first distance. --

IN THE DRAWINGS:

Figs. 1 and 2 have been amended in response to objections raised by the Examiner.